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Smart-Cut: A New Silicon On Insulator Material Technology Based on Hydrogen Implantation and Wafer Bonding*

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An alternative route to existing silicon on insulator (SOI) material technologies such as SIMOX (separation by implanted oxygen) and BESOI (bonded and etch-back SOI) is the new Smart-Cut process, which appears to be a good candidate to achieve ULSI criteria. The Smart-Cut process involves two technologies: wafer bonding and ion implantation associated with a temperature treatment which induces a in-depth splitting of the implanted wafer. The details of the Smart-Cut process, the physical phenomena involved in the different technological steps such as hydrogen implantation related mechanisms and wafer bonding are discussed. The characteristics of the final structure in terms of thickness homogeneity, crystalline defects, surface microroughness, and electrical characterization are presented. Other applications of this process are also highlighted.

KEYWORDS: silicon on insulator, wafer-bonding, smart-cut, hydrogen implantation

1. Introduction

Up to now silicon on insulator (SOI) technology developments were mainly geared to radiation-hardened electronics for military and space applications. Today, SOI technologies appear to be a key issue for low-power, low-voltage electronics, and should play a major role in future ULSI developments.[1)] One of the key issues for development of SOI-based microelectronics is the availability of good-quality, low-cost SOI material in suitable quantity. Among the many SOI material technologies developed during the past two decades, SIMOX (separation by implanted oxygen) has reached the level where industrial companies are able to offer standard specified products on the market, and for the past few years there has been a growing interest in SOI material technology based on wafer bonding and etch back (BESOI).[2,3)] For achieving thin uniform SOI layers the BESOI technology involves either an etch stop layer or a combination of accurate thickness mapping and fine local thinning with a localized plasma.[4,5)] In addition to these processes the new Smart-Cut SOI process involves the best features of the implantation and wafer bonding technologies for production of Unibond[6)] wafers. Implantation enables a high degree of uniformity of the top silicon layer to be obtained whereas the wafer bonding step enables the good crystal quality of the silicon wafer to be preserved. This process, taking advantage of its unique splitting effect, appears to be an alternative route, able to meet the criteria necessary for development of ULSI technologies: thickness homogeneity, good crystalline quality, low cost, and availability.

The Smart-Cut process[7,8)] basically comprises four main steps (Fig. 1):

—Step 1: Hydrogen implantation into a wafer A capped with a dielectric layer, thermally grown SiO_2 for example (dose in the 3.5×10^{16} to $1 \times 10^{17}\,cm^{-2}$ range)

—Step 2: Hydrophilic bonding at room temperature of wafer A to a handle wafer B (wafer B is either bare or capped). Both wafers are previously cleaned using a modified RCA process. Wafer B plays a key role in the Smart-Cut process as a stiffener and provides the bulk silicon under the buried oxide in the SOI structure.

—Step 3: Two-phase heat treatment of the two bonded wafers. During the first phase (400–600°C) the implanted wafer A splits into two parts: a thin layer of monocrystalline silicon remaining bonded to wafer B thus giving rise to a SOI structure, and the remainder of wafer A. The second high temperature treatment phase (around 1100°C) strengthens the chemical bonds.

—Step 4: Touch polishing-after splitting, the layer of the SOI structure exhibits micro-roughness which makes polishing of the surface necessary for elimination of the disturbed region.

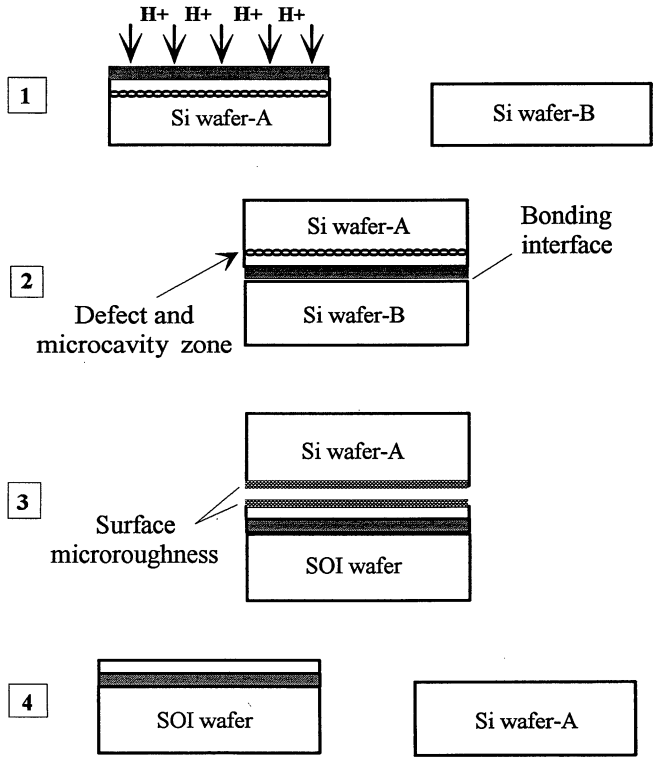

Fig. 1. Principle of the Smart-Cut process.

*Smart Cut is a registered trademark of SOITEC.

Noteworthy: Wafer A whose surface layers ($Si+SiO_2$) have been removed by the splitting process can be recycled using touch polishing to be used as wafer B in a subsequent process flow.

2. Hydrogen Implantation and Splitting

High dose inert gas or hydrogen implantation in materials can induce visible macroscopic effects such as blistering, swelling, flaking and exfoliation. These effects have been known for a long time.[9,10] This is a major issue for design of thermonuclear reactors where extensive damage to the inner wall of the reactor occurs due to helium ion bombardment.[11]

The possibility of making silicon flakes using hydrogen or inert gas ion implantation into silicon opens up the way for a new SOI material technology. The challenge involves increasing the flake area by a factor of about 10^8 ($100\,\mu m^2$ to full wafer), keeping the crystalline structure of the layer defect-free (especially preventing the layer from being subjected to stresses leading to plastic deformation).

Due to the small amount of damage induced by implanted hydrogen ions (most of the stopping power is due to inelastic scattering), the relatively moderate ion fluences, and self-annealing of defects during implantation, it appears that silicon flakes originating from single-crystal silicon can be prevented from undergoing irreversible damage.

For silicon, blistering and flaking (Fig. 2) can be obtained in two ways:

—Firstly: by performing high-dose implantation. In this case blistering becomes visible for doses of around $2\times10^{17}\,cm^{-2}$, and flaking occurs as the dose is increased.

—Secondly: by performing medium-dose implantation and annealing. The first step consists of achieving limited hydrogen dose implantation (around $3\times10^{16}cm^{-2}$ to $1\times10^{17}\,cm^{-2}$). The second step consists of performing a thermal treatment (400°C to 600°C) resulting in blistering and flaking. These effects are associated with in-depth microscopic defects. Transmission electron microscopy (XTEM) cross sections show microsplits extending parallel to the surface (Fig. 3). It is noteworthy that the surface quality after step one is sufficient to enable bonding of the implanted surface to another wafer.

The originality of the Smart-Cut process is to use the basic physical phenomenon related to blistering, i.e. creation of microcavities containing a gas phase, as a way of inducing in-depth splitting at the end of the range of implanted protons over the whole wafer.

In the Smart-Cut process, the handle wafer is bonded to the implanted wafer and acts both as a stiffener and as a support for the transferred layer. Stiffening of the upper layer must be understood as attaching it to a substrate or layer with appropriate mechanical properties. This can be achieved by deposition of thick and adherent layers on the surface or by bonding of a substrate to the surface.

As the need for very flat surfaces is a key issue in wafer bonding techniques, the possibility of keeping the surface free from any deformation or even blisters after the implantation step appears to be of prime importance. It is in the medium dose implantation case in which no defects are observed at the surface whereas some microscopic defects are present in the silicon. High-resolution XTEM observations of as-implanted samples show microcavities located at a depth corresponding to the projected range, oriented following the (111) and (100) planes for (100) silicon wafers (Fig. 4).

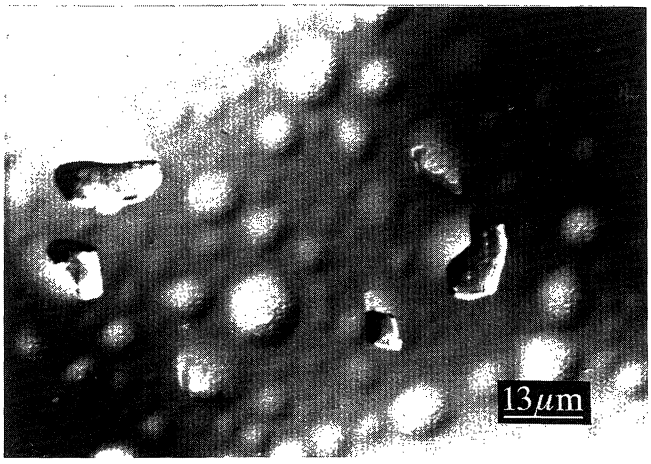

Fig. 2. Blistering and flaking at the silicon surface.

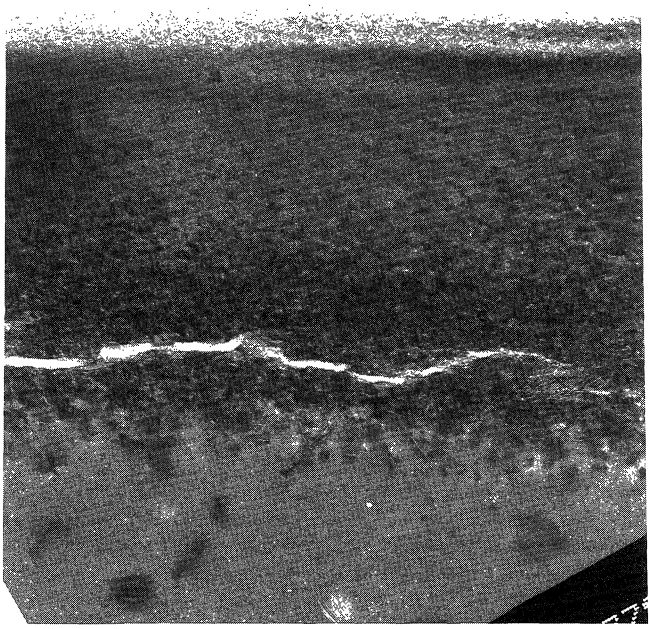

Fig. 3. TEM cross section of a crack in silicon after hydrogen implantation and annealing.

The mean size of the microcavities increases during annealing (Fig. 5) leading to the formation of a crack parallel to the bonded surface. This crack propagates along the large microcavities which are distributed within a layer whose thickness is about ΔR_p (projected range straggling). So after splitting, a high degree of surface microroughness is obtained (12 nm RMS) (Fig. 6).

To summarize, medium dose hydrogen implantation into silicon induces microsplitting during annealing at a depth corresponding to peak hydrogen concentration.

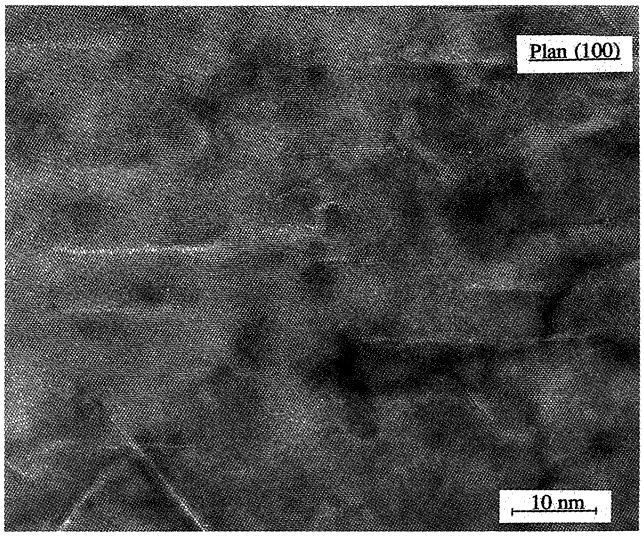

Fig. 4. High resolution TEM cross section of microcavities on hydrogen-implanted silicon.

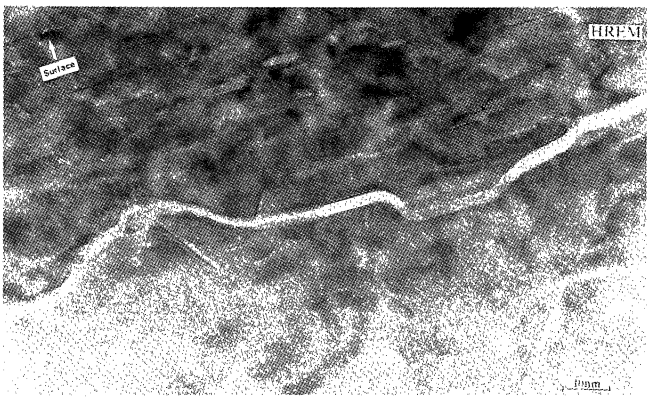

Fig. 5. High resolution TEM cross section of microcavities on hydrogen-implanted silicon after low-temperature annealing.

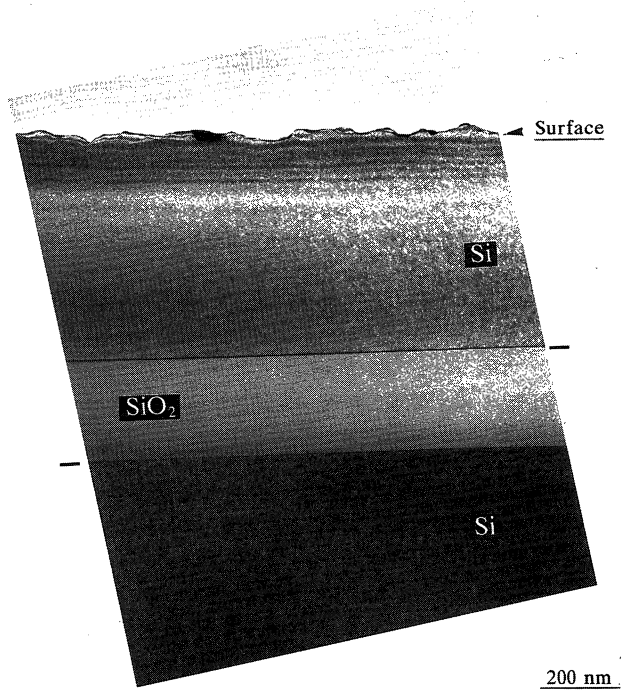

Fig. 6. SOI structure after in-depth splitting.

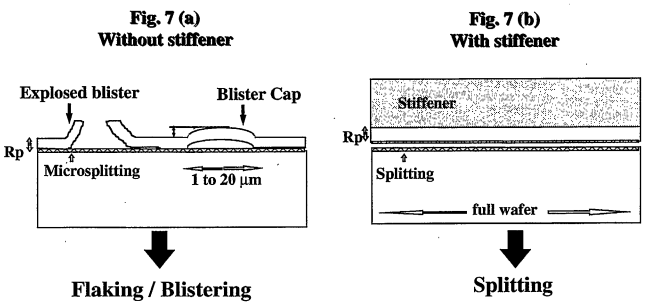

Fig. 7. Schematic of the effect of hydrogen implantation into silicon a) without stiffener, b) with stiffener.

However, this microsplitting develops differently depending on the conditions at the wafer surface; i.e. (Fig. 7),
—if the surface is free (without stiffener), during annealing the microsplitting induces deformation of the thin film and blisters appear at the surface.
—if a stiffener is present on the surface, deformation of the thin film is impossible and the microsplitting induces splitting of the full wafer.

3. Cleaning and Bonding

For achieving high-quality bonding, the contacting wafers must be scratch-free and cleaned to remove any particle or organic contamination. Microroughness also influences the bonding and must be lower than 0.5 nm RMS.[12] For formation of the SOI wafer, hydrophilic conditions are used to bond the implanted oxidized wafer to the silicon handle substrate. The Smart-Cut process requires specific cleaning conditions before bonding because the implantation step modifies the oxide surface in terms of particle and organic contamination. The particle contamination density is monitored using a 6200 Tencor Surfscan on the largest area. Using a 2 mm exclusion

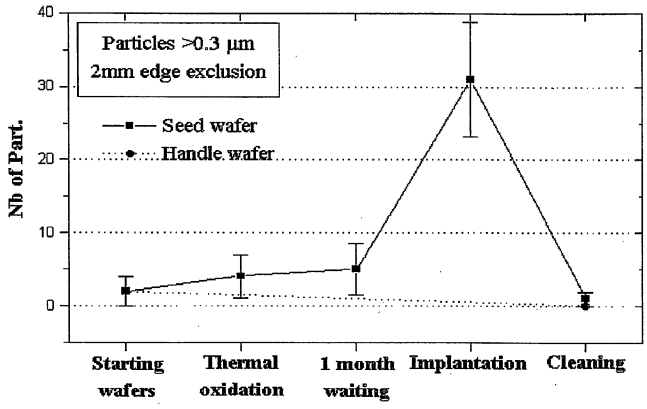

Fig. 8. Monitoring of the particle contamination density throughout the Smart-Cut process.

area, it is possible to detect particles responsible for specific defects on the edge of wafer bonding products. Figure 8 shows the evolution of the particle contamination

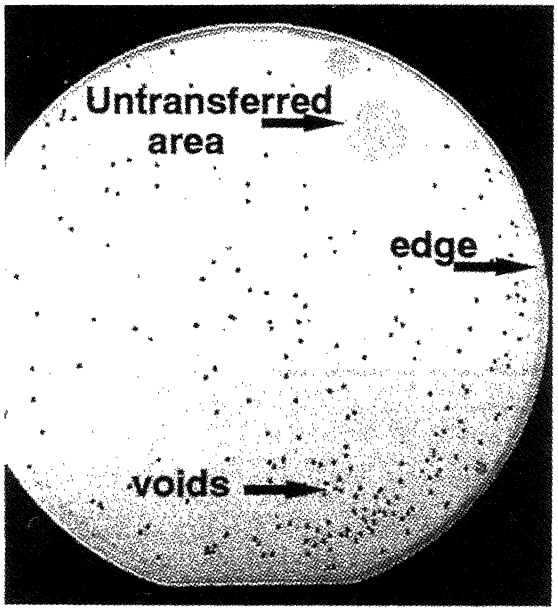

Fig. 9. Magic mirror view of the SOI structure obtained after splitting with standard cleaning.

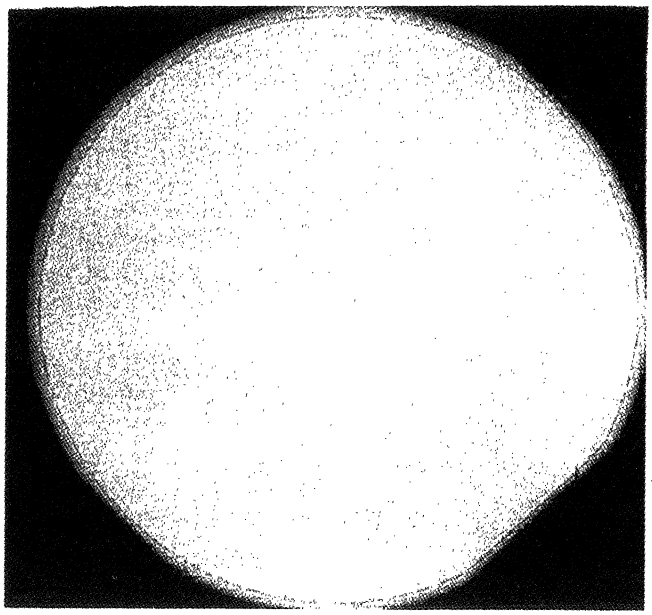

Fig. 10. Magic mirror view of the SOI structure obtained after splitting with modified RCA cleaning.

density on both wafers throughout the process. Whereas the particle contamination density is very low on initial and oxidized wafers, implantation induces contamination and the density reaches 0.5 particles/cm^2.

In the same way, the chemical state of the oxide surface was checked throughout the process using the contact angle measurement method with a water droplet placed on the surface. Results of measurement of the contact angle give an indication of the surface stress and of the hydrophilic state of the surface.[13] Once again, the implantation step is responsible for most of the degradation of the hydrophilic state, the contact angle values increasing from 20–30° (on an oxidized wafer) to 50–65° (after implantation). This change is due to organic surface contaminants identified as hydrocarbons using MIR-FTIR spectroscopy.[14]

So, in the case of unoptimized cleaning, macroscopic defects can be detected just after the first annealing step, i.e, the splitting step (Fig. 9).

—Untransferred zones: large particles induce formation of an unbonded area, resulting in an effective local lack of stiffening effect, thus preventing the splitting from occurring in this area.

—Microvoids: particle and hydrocarbon contamination induces microvoid formation at the bonding interface. These small defects tend to inflate during annealing as soon as the splitting occurs, resulting in plastic deformation of the SOI surface.

—The bevelled edge of commercial wafers prevents bonding from occurring in a ring area about 1.5 mm wide and influences the adhesion over a few millimeters. This effect combined with particle contamination induces formation of the last type of macroscopic defect, small edge defects observed on SOI wafers.

All these defects are clearly visible by magic mirror view observation (Hologenix equipment).

For avoiing the formation of such defects, a specific cleaning procedure using a modified RCA process was developed. After implantation, the bonding capability of the oxide surface is restored, almost no particle of a size larger than 0.3 μm is trapped between the wafers at bonding, and the bonding site density (OH groups) is rather high, resulting in a high bonding wave velocity estimated to be in the range of 3–4 cm/s using IR transmission observation. This specific cleaning yields a final SOI structure free from macroscopic defects, as revealed by magic mirror view observation (Fig. 10).

4. Characterization of the SOI Structure

The SOI structure exhibits uniformity of the silicon layer thickness better than 10 nm min-max over 100 mm wafers. Surface microroughness is also a key parameter because of its impact on the gate oxide breakdown voltage. In addition to mean (1.2 Å) or RMS (1.5 Å) values, power spectral densities were investigated by AFM to check that Unibond wafers have a morphological surface structure quite similar to that of bulk silicon.[15]

For assessment of the crystalline quality of the silicon layer, chemical characterization was carried out using a four-step Secco etch. An etch pit density ranging from 10^3 to 3×10^4/cm^2 was measured for 50 nm of silicon remaining after the first etch. SEM observations of the etch pits showed an unconventional shape for crystal defects. For checking of the density of crystalline defects, epitaxy was carried out on the SOI wafer. A Secco etch showed a very low defect density of about 20 defects/cm^2, identified as threading dislocations through the SOI layer. No stacking faults or slip lines were observed over wafers both before and after epitaxy demonstrating a very high crystal quality of the final SOI material. Moreover, a 50% HF solution etch for 15 min revealed an etch pit density of about 1/cm^2.

The electrical behavior of the SOI structure was evaluated using a pseudo-MOS transistor.[16] Doping of the

silicon film is p-type and its concentration was measured as $5 \times 10^{15}/cm^3$. The interface state densities and mobilities were found to be as good as for the best SOI materials.

ULSI electronic devices made with ultra thin gate oxides (4 nm) have demonstrated interesting electrical behavior. The breakdown intrinsic field was measured at about 15 MV/cm on both SOI wafers and the best silicon materials. *I-V* measurements on capacitors of various sizes show that no pinhole or conductive defects exist in the buried oxide of the Unibond wafers.

5. Main Characteristics of the Smart-Cut Process and Advantages

5.1 *Layer thickness uniformity*

One of the benefits of the Smart-Cut process is the flexibility of the thicknesses of both the buried oxide and the silicon layers. The buried oxide layer is thermally grown and its thickness can be tuned with high reliability. The silicon upper layer of the SOI structure is obtained by splitting at the depth of maximum concentration of hydrogen (R_p). The SOI structure thicknesses (Si thickness, SiO_2 thickness) are directly related to the ion energy through the relationship between the depth of maximum concentration of hydrogen (R_p) and implantation energy (rate of about 8 nm/keV in silicon-Fig. 11), with no evidence of a dose effect.

The ion energy is accurately and easily controlled, so the layer thickness after splitting is inherently homogeneous (dispersion min-max <4 nm).

5.2 *Crystalline quality and interface quality*

Using medium implantation doses and light ions minimizes atomic displacements giving rise to high crystalline quality SOI layers. Moreover, roughly one-half of the disturbed zone in the vicinity of R_p is separated from the layer by the splitting process, and the other half is suppressed by the final polishing.

The Smart-Cut technology provides a very high-quality front interface (interface between the upper silicon layer and buried oxide). More precisely, the process is compatible with a front interface: silicon-thermally grown oxide, which guarantees the lowest interface state density. Due to the high penetration capacity of protons, it is possible to fabricate the buried dielectric layer through thermal oxidation at the very beginning of the process and then perform hydrogen implantation through this SiO_2 layer, even if it is rather thick. This is a great advantage when compared with the BESOI technology using etch-stop layers. In this case, keeping the etch-stop properties is hardly compatible with the thermal budget associated with the buried oxide thermal growth.

5.3 *Industrial aspects*

All the basic steps involved can be performed on standard microelectronics facility equipment. Implantation is performed on standard high-current machines designed for source-drain or polysilicon doping. Heat treatments can be performed in standard furnace tubes; cleaning is performed on wet-bench or wet cleaning machines designed for ULSI technology, and in the last polishing step the same machines as for bulk wafer final polishing or chemical-mechanical polishing of inter-level dielectrics are used.

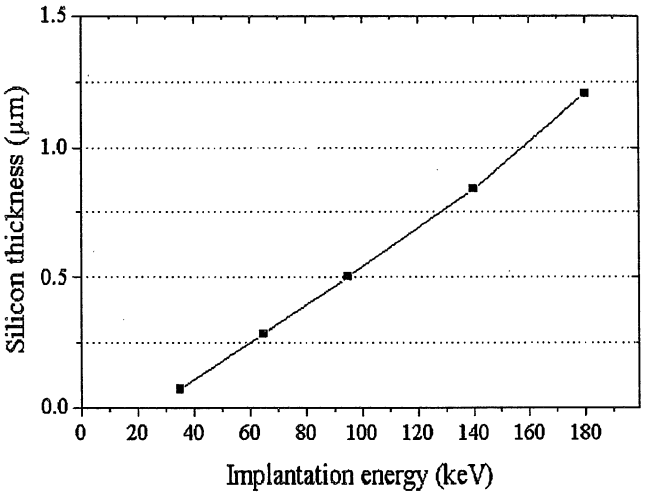

Fig. 11. Variation of the silicon layer thickness versus implantation energy for 400 nm thick oxide.

When compared with the SIMOX process, the Smart-Cut process presents the advantages of being based on a more "comfortable" and easier to industrialize process. Among the advantages, the following should be specially pointed out: for the Smart-Cut process the ratio of the dose range is up to fifty times less than that for SIMOX. Annealing treatments can be performed in classical furnaces instead of the specially designed very high temperature (1320°C) furnaces used for the SIMOX process.[17]

Moreover, an additional economic advantage of the Smart-Cut process over BESOI technologies is apparent: no wafer is wasted in grinding operations and one SOI wafer is obtained for one bulk silicon wafer whereas in BESOI technologies two wafers are needed to obtain one SOI wafer.

5.4 *High potential*

The principle of the Smart-Cut process is suitable for different kinds of applications:

—Single-crystal silicon films can be transferred onto any kind of substrate provided that this kind of substrate can be bonded to silicon and that the bonded structure can withstand temperatures in the 400°C–600°C range. Interesting results on single-crystal silicon on glass or quartz for display applications have been obtained.

—More generally, the principle of the Smart-Cut process applies to applications involving fabrication of single-crystal semiconductor films and their transfer onto different kinds of substrates. At LETI the process was applied successfully to silicon carbide[18] for making silicon carbide on insulator with a SiC monocrystalline layer 200 nm thick around 1000 nm of deposited oxide as insulator and either polycrystalline SiC or bulk silicon wafer as the underlying substrate. Other studies are planned for assessing the compatibility of the process with III–V semiconductors.

—The process also applies to transfer of structured and

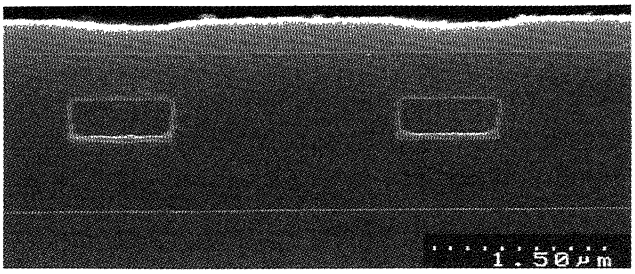

Fig. 12. SEM observation of the cross-section of the patterned film after transfer.

patterned layers[19] or even transfer of electronic devices. The key issue for this kind of application is the compatibility of the process with non-homogeneous layers, i.e., the possibility of inducing continous splitting over the entire surface even if the microcavityes layer comprises discontinuous parts at different depths due to the structures of the various layers and the different compositions the proton beam encounters (Fig. 12). It was demonstrated that the process can be applied without any problem, provided that variations of the penetration depth remain lower than 100 nm: this is not a large constraint in the case of layers composed of SiO_2 patterns, Si patterns and Al patterns; all these materials exhibit similar behaviors with respect to ion penetration due to the similarities of their atomic number.

6. Conclusion

The Smart-Cut process appears to be highly suitable for making high-quality SOI wafers with the great advantages, related to the intrinsic properties of light ion implantation, of low defect density and thickness homogeneity. All the basic steps involved can be performed on standard microelectronics equipment. The Smart-Cut process could be the way to fabrication of a less expensive but high-quality SOI material giving rise to rapidly increasing penetration of SOI technologies into the advanced mass production market.

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